# Organization of Digital Computers LAB EECS112L

Lab2: Single cycle processor

1/30/2021

## 1 Objective

In this project, I modified and improved the code for a single cycle processor given by the instructor.

## 2 Procedure

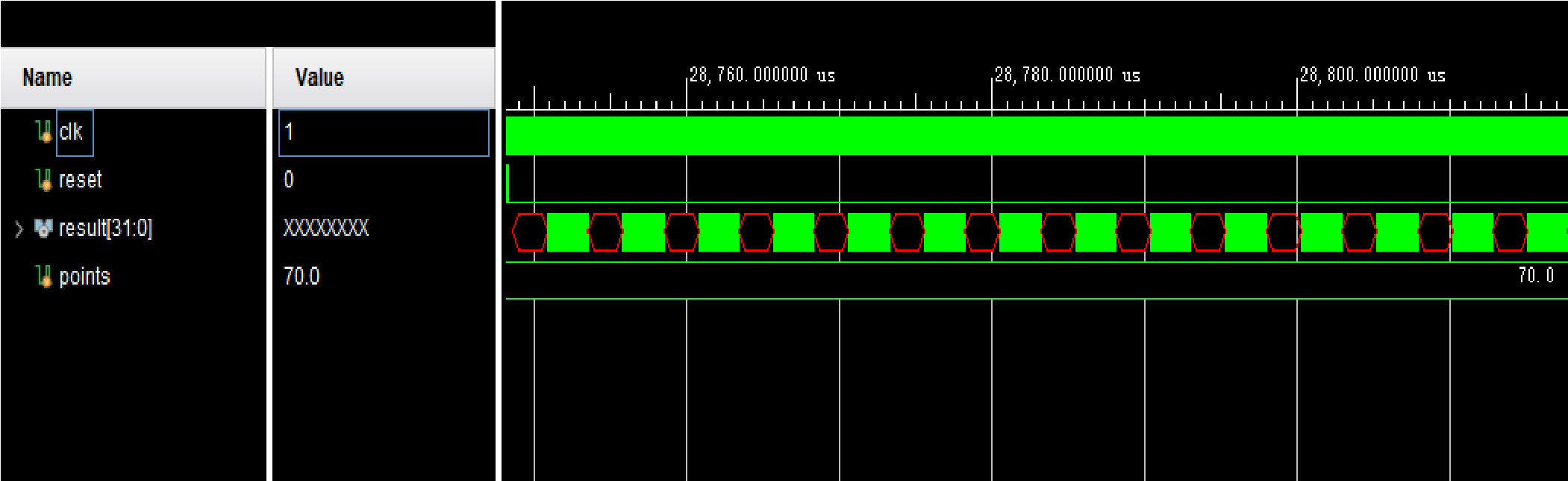
The given code is already almost perfect. However, there were still some missing instructions and connections.

Firstly, I noticed that in the Datapath, several wires and components were missing. Specifically, shift left 2, branch\_mux, the and gate connecting branch and alu\_zero. Then, I added those components and wires in Datapath.

Next, I needed to add more instructions as specified in the lab manual. I went to the alu module. Under always statement, I added other instructions based on various alu\_control, such as div, sra, sll, srl, nor, add, etc.

Then, I went to the alu\_control module. In order for the alu to implement instructions correctly, the number of alu\_control signals needed to be increased. Therefore, I combined ALUOp and Function as input, regarded alu-control as an output, and add the code for according instructions according to table 4 in the lab manual.

Finally, I went to the control module. I found that there were also missing code. I then added the code for srl/slt/sll, andi, beq,and jump instructions.



## 3 Simulation Results

I used the given tb, and all the results were correct as expected.